

Figure 1A
Prior Art

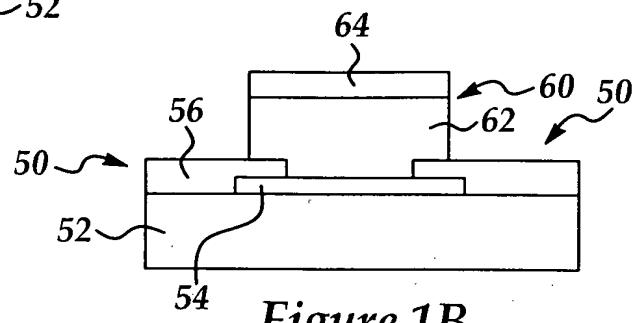


Figure 1B
Prior Art

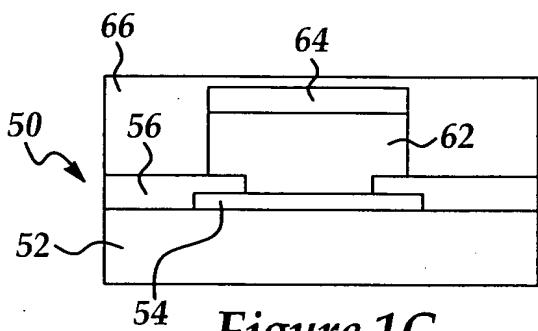


Figure 1C
Prior Art

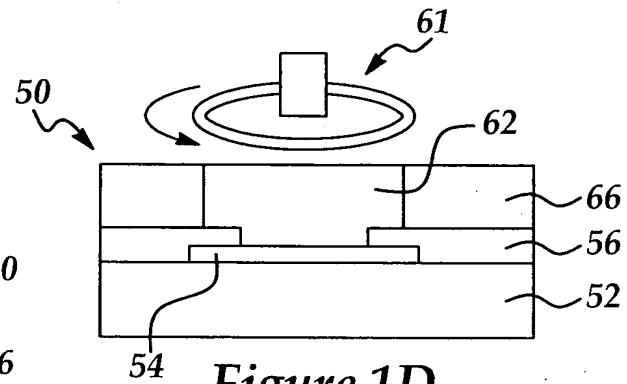


Figure 1D
Prior Art

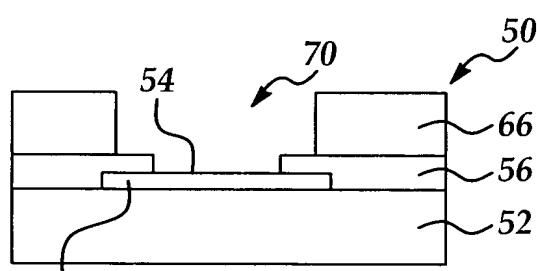


Figure 1E
Prior Art

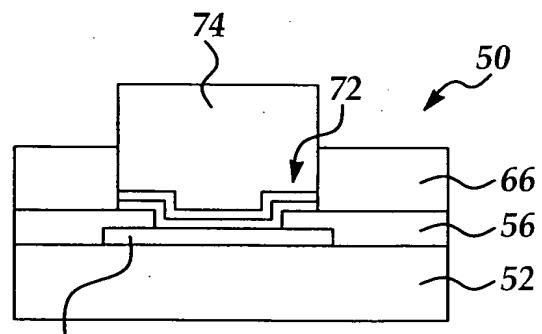


Figure 1F
Prior Art

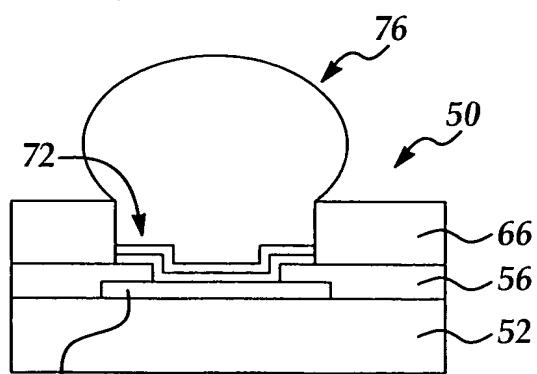


Figure 1G





Inventor: Hsin-Hui Lee
Serial No.: 10/045,783 Filed: 01/12/2002
For: Method of Making a Wafer Level Chip Scale Package
Attorney Doc. No.: 67,200-591

2/5

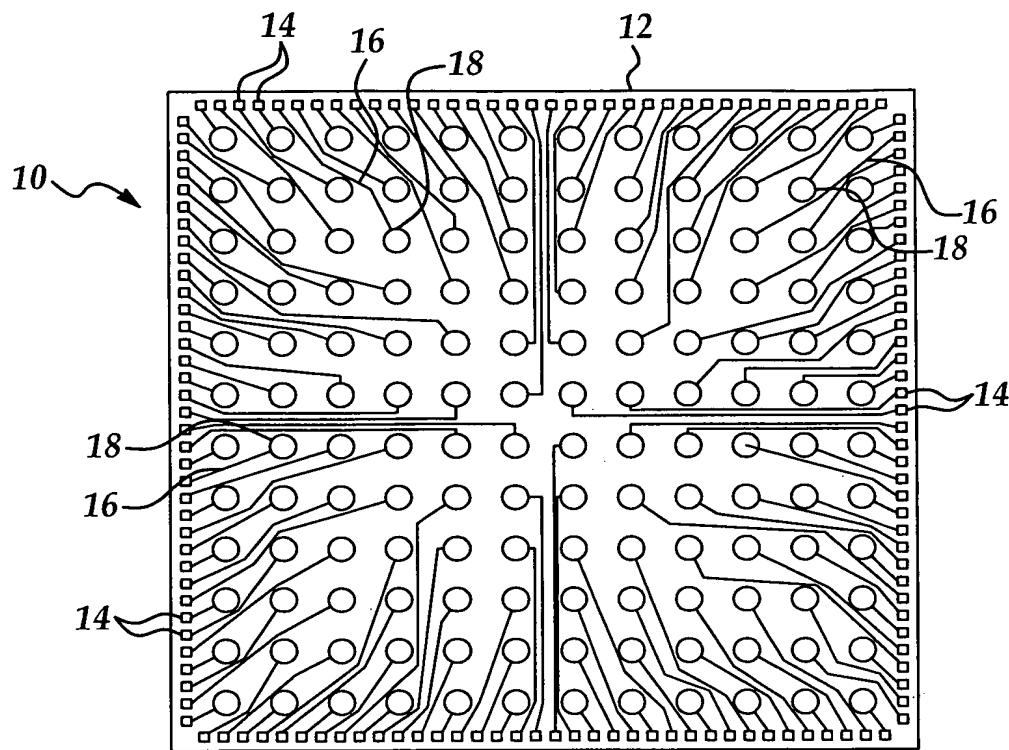


Figure 2
Prior Art

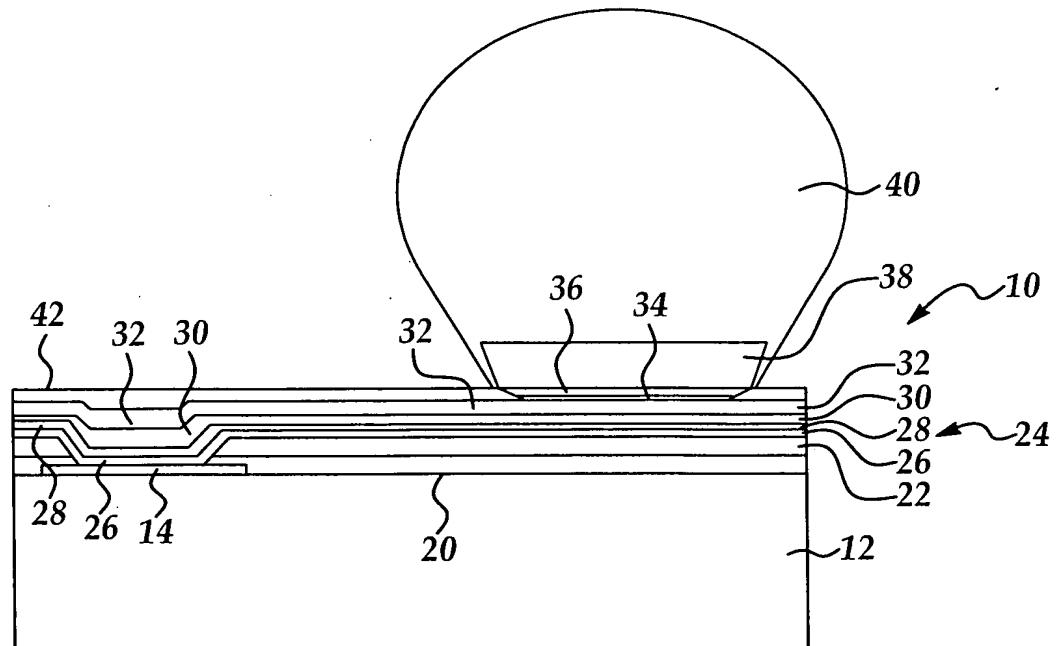


Figure 3
Prior Art

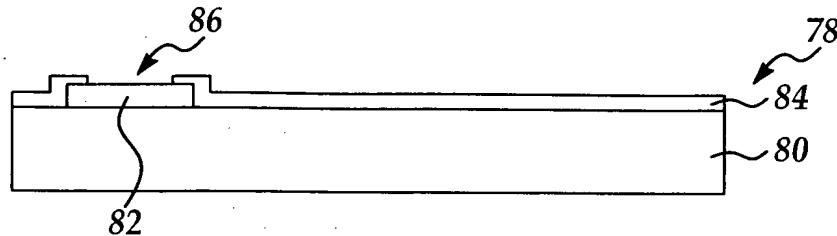


Figure 4A

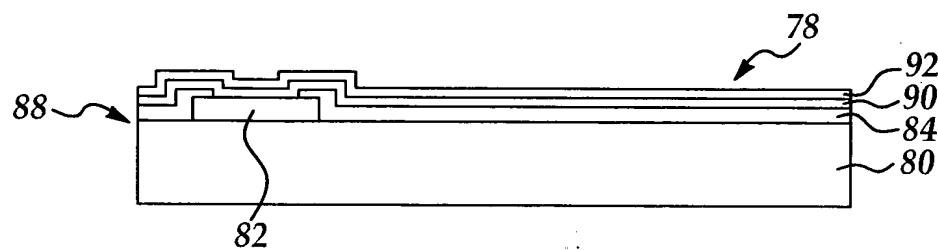


Figure 4B

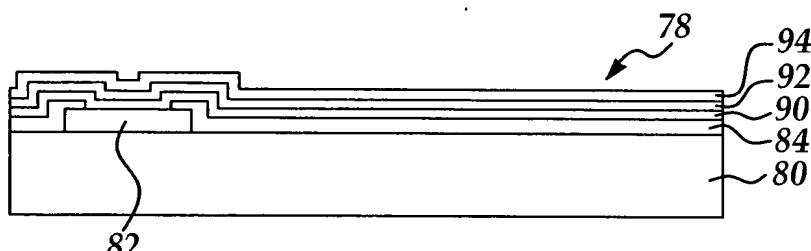


Figure 4C

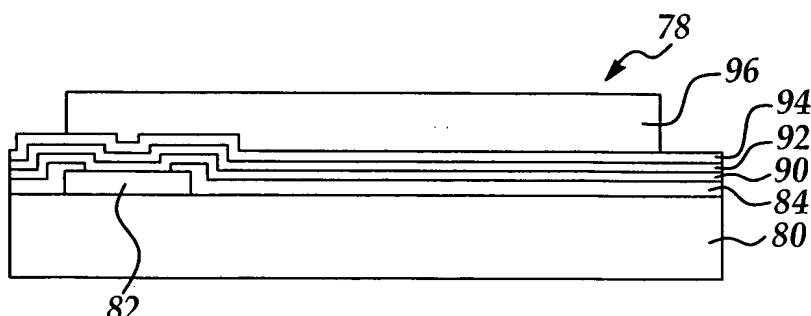


Figure 4D

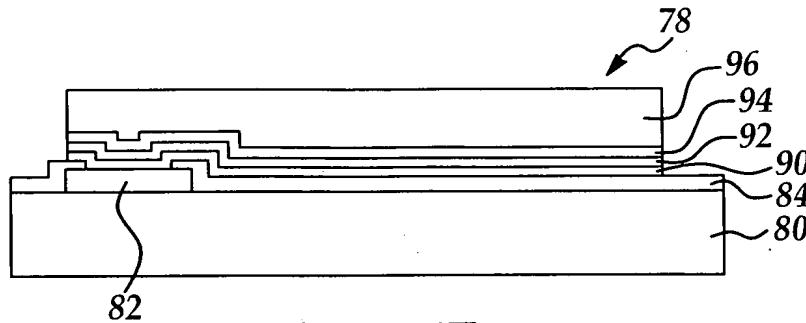


Figure 4E

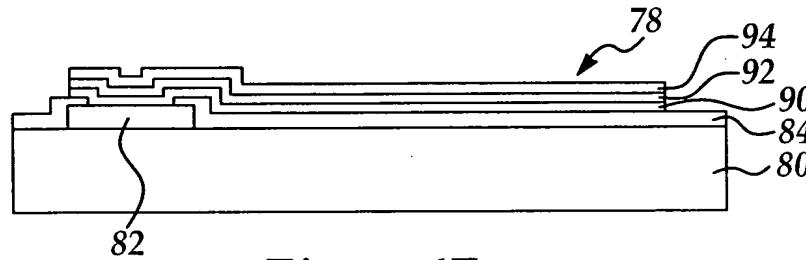


Figure 4F

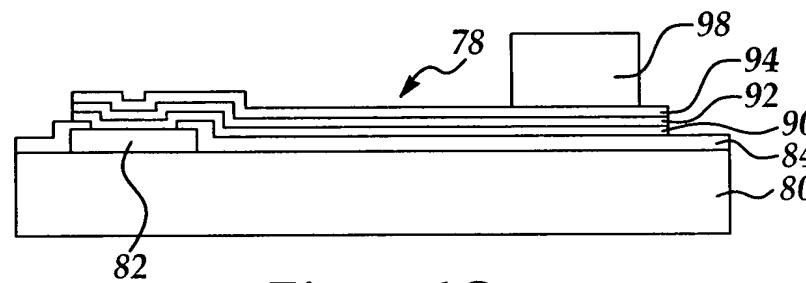


Figure 4G

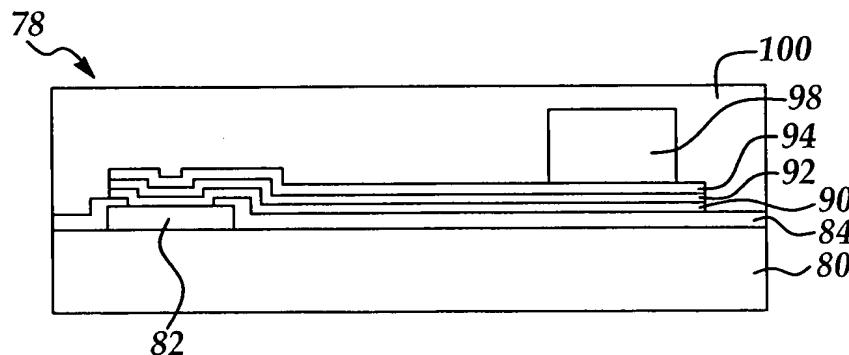


Figure 4H



Inventor: Hsin-Hui Lee
Serial No.: 10/045,783 Filed: 01/12/2002
For: Method of Making a Wafer Level Chip Scale Package
Attorney Doc. No.: 67,200-591

5/5

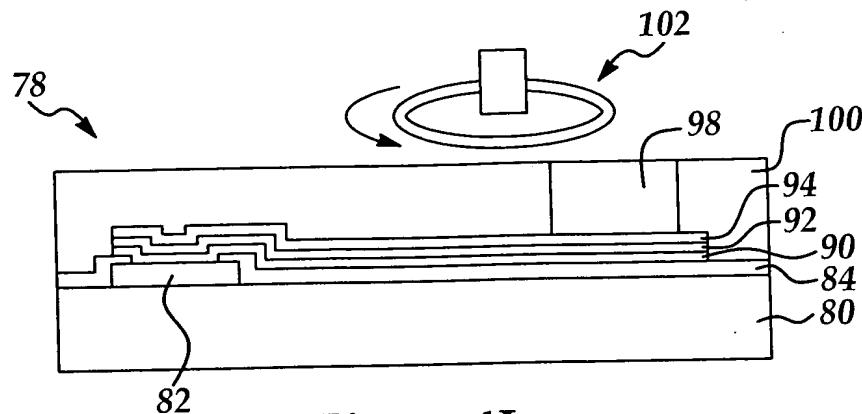


Figure 4I

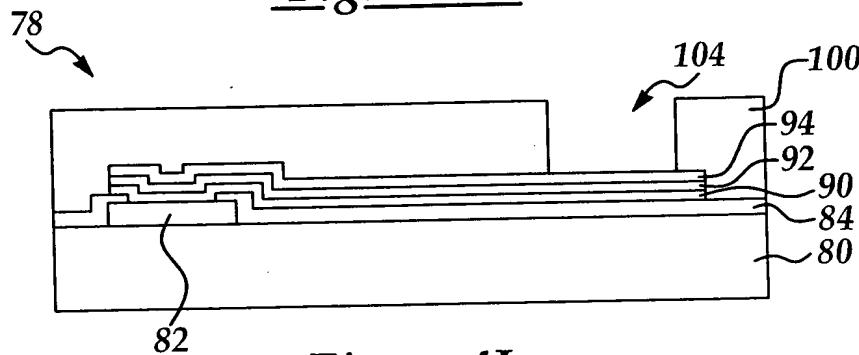


Figure 4J

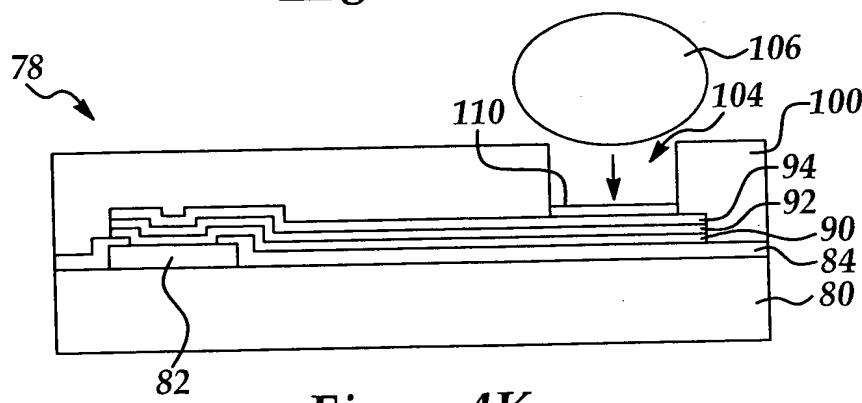


Figure 4K

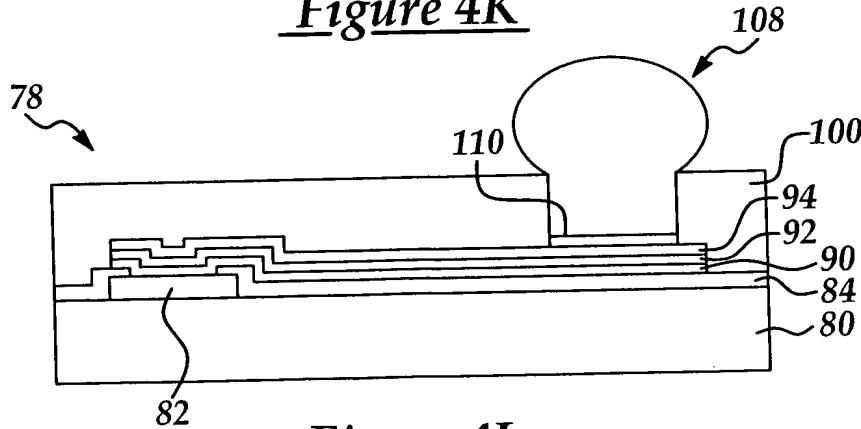


Figure 4L